Review of procedures to overcome spurious effects in the measurement of RF communication cables

Laurent Van Rysselberghe, Wolfgang Klein, Dick Gigon, Boris Dardel, V. Arbet-Engels

AESA SA

Colombier, Neuchâtel, Switzerland

+41-32-843-3684 · lvrysserberghe@aesa-cortaillod.com

Abstract

With the advance of multigigabit data rate communications needed to sustain the ultra-high bandwidth of Internet of things (IoT), the electrical characterization of cables is becoming paramount. These cables must comply with international standards that not only set RF parameter limits but also define measurement procedures.

These measurements can be done either in the frequency or time domain. Using Fourier transformation allows converting from one representation to the other.

Nevertheless, one of the main challenges is to isolate the DUT (Device Under Test), the cable in our case, from the rest of the measurement environment in order to get its intrinsic characteristics. As a matter of fact, the DUT is connected to the ATE (Automatic Test Equipment) via interfaces with their own frequency response that must be removed from the DUT itself. Additionally, at high frequency, the measurement is becoming extremely sensitive to the way the operator is connecting the DUT on the ATE, with parasitic effects that directly impact the accuracy and/or precision of the measurement (repeatability/reproducibility).

Keywords: Transmission lines; impedance; return loss; Vector Network Analyzer; data cable; S-parameters; S_{11}.

1. Introduction

Given the large amount of parameters to be measured and calculated, data cable characterization is performed using fully automated test equipment (ATE). However, the obtained data strongly depend on the test setup, the calibration, the DUT preparation, and other parasitic effects. It is thus required to carry out some corrections on the basis of theoretical principles in order to extract the DUT intrinsic return loss and/or impedance.

In this paper, we review various correction procedures to remove the influence of the operator in the cable preparation on the DUT characterization, as well as mismatch effects of cable fixtures. In the first and second parts, we re-visit the theory of transmission line and then describe the measurement principle. In the third and fourth parts, we review correction procedures, first in the frequency domain and then in time domain, and discuss their respective advantages and disadvantages. In the last part, we discuss de-embedding as a means to remove the effect of the test fixtures.

2. Transmission Line Basic Parameters

To begin with, let's briefly come back to the basics of transmission line theory in order to seize the complexity of data interpretation.

The characteristic impedance of a transmission line (i.e. the cable in our case) as function of the primary parameters is expressed as follows:

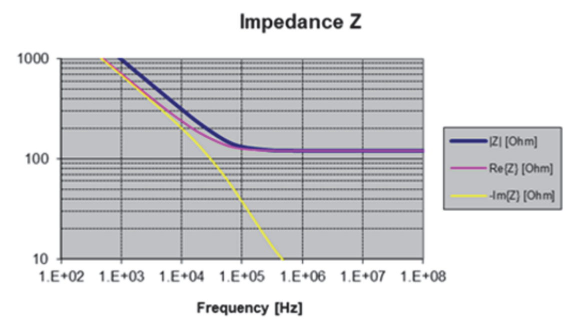
$$Z_c = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{1}$$

Similarly, the complex propagation constant is given by the following formula:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L) \times (G + j\omega C)} \tag{2}$$

with the real part α and β being the attenuation and phase constant, respectively.

For a twisted copper pair, these parameters are illustrated in Figure 1 below.



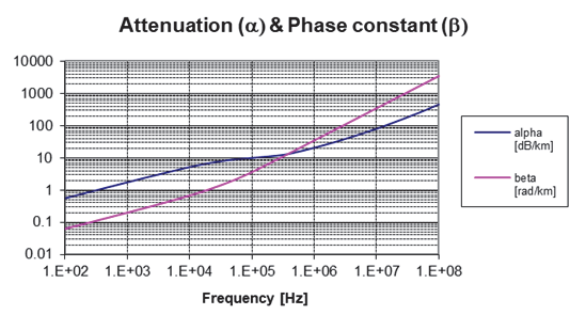


Figure 1: Characteristic impedance and propagation constant for a twisted copper pair cable

At high frequency, the impedance levels off to an asymptotic value close to $\sim\sqrt{L/C}$, with its imaginary parts fast decreasing to zero. The observed kink on the curves at f ~100 KHz is mainly due to the skin effect becoming dominant at high frequencies.

These parameters can be extracted from test measurement using an ATE as described in the following section.

3. Measurement Principle

An ATE consisting of a VNA (Vector Network Analyzer), a switch matrix and a cable interface is capable of measuring directly the complex reflection/transmission coefficients (S-parameters) of the DUT. The typical setup is depicted below.

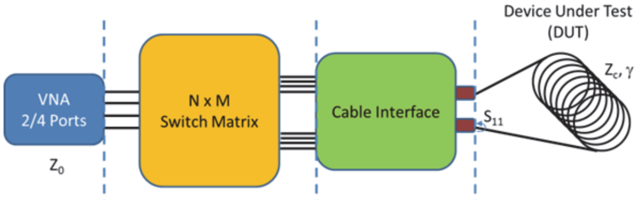


Figure 2: Schematic of an ATE, with the VNA, switch matrix, cable interface, and DUT

Cable parameters are directly related to complex S-Parameters (scattering parameters). In particular the characteristic impedance of the cable is related to S_{11} as follows:

$$Z_c = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \tag{3}$$

with the return loss defined as:

$$Return\ Loss(RL) = -20\, log_{10}(|S_{11}|) \quad [dB] \tag{4}$$

where S_{11} is the ratio of the reflected voltage wave to the incident voltage wave.

In order to have the calibration plan at the DUT, a so called "zero correction" is performed, using for instance the popular full 2/4 ports SOLT (Short-Open-Load-Through) procedure. Depending on the cable interface type, a de-embedding calculation might be used to remove cable interface influence on the overall frequency response. It is worth noting that it is technically challenging to do the mathematical de-embedding of the cable interface along with the accurate SOLT calibration over the full frequency range.

The measurement of a cable will be influenced by the following various effects that need to be individually identified for proper data analysis.

1. Intrinsic structural defects of the cable
2. Impedance mismatch at both cable ends
3. Effect of cable preparation
4. Calibration related effects

For the cable manufacturers, what is sought for is the identification of the structural defects and thus to sort out these latter from the other ones for continuous improvement in quality of their production process.

The impedance mismatch at both ends of the cable will result in multiple reflections specifically at low frequencies where the round trip attenuation is less severe than at high frequencies.

At high frequencies, the cable end preparation will perturb the measurement due to unwanted stray capacitances and inductances.

And last but not least, a calibration with SOLT artefacts not perfectly mimicking the cable fixtures will lead to errors and render the interpretation of the data cumbersome.

Models based on physical understanding of these effects and measured data can be used to interpret or extract the relevant cable parameters. As an example, the simulation of the effect of reflexions on a non-terminated ("Open") cable is shown in Figure 3.

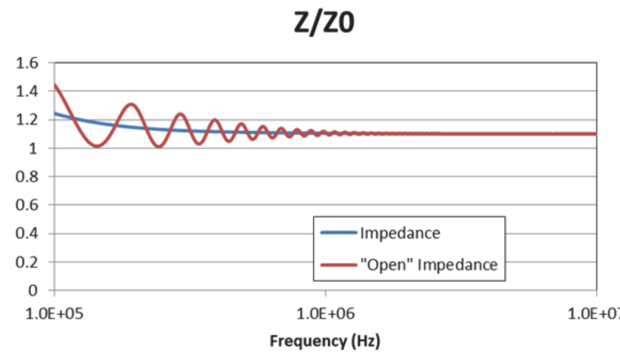


Figure 3: Calculated impedance and simulated "Open" impedance for a copper pair

The oscillations associated with the reflection at the cable "Open" far end are visible, illustrating the difficulty at extracting the correct impedance value of the DUT.

Different methods and correction procedures have been defined by standards to assist in data analysis. Among these, we can list:

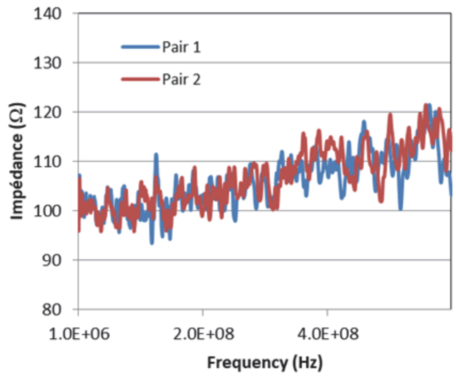
- Open/short method to remove impedance mismatch at cable far end (IEC/TR 62152)
- Structural return loss method, based on open/short measurement, to remove impedance mismatch at near end (IEC/TR62152)
- Parasitic inductance correction to removes stray inductances at cable fixture
- Gating to remove cable connectors' effects

In the following sections, we discuss these approaches, their respective advantages and disadvantages, based on experimental test measurement with ATEs. It includes both frequency and time domain analysis, respectively.

4. Frequency Domain Analysis

4.1 Function Fitting of the Magnitude of the Characteristic Impedance (IEC 61156-1-2)

Figure 4 shows measured (top) and fitted (bottom) impedance curves for a twisted pair cable (2-pairs) from 1MHz up to 6MHz.



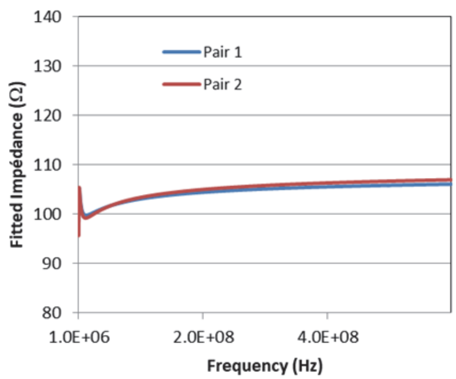


Figure 4: Measured and fitted impedance

Contrary to expectations, the impedance does no tend to an asymptotic value but keeps increasing at higher frequencies. Reasons for this could be multiple, among which the spurious effects highlighted in the previous section.

At the bottom of Figure 4, the impedance is fitted with a least square method according to the following 4-coefficients equation:

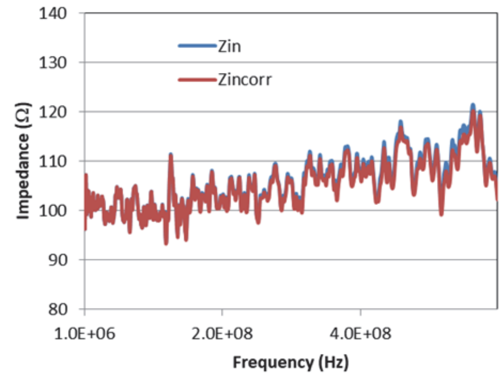
$$|Z_C| = K_0 + \frac{K_1}{\sqrt{f}} + \frac{K_2}{f} + \frac{K_3}{\sqrt{f^3}} \quad (5)$$

where K_0 represents the external space inductance and capacitance of the pair; K_1 the internal inductance; K_2 and K_3 higher order effects.

Least square fit gives a smooth curve that roughly represents the value of the impedance as function of frequency. It removes the effect of the structural defects of the DUT and allows making a comparison with the expected and/or specified value of the impedance. In our present case, where the impedance increases with frequency, the curve fit deviates from the expected shape shown in Figure 1 and Figure 3.

4.2 Parasitic Inductance Correction (IEC 61156-1-5)

Cable preparation and the way operator will connect the cable to the cable fixture/interface could add parasitic inductances and or capacitances with undesirable effect on the measurements. This could partly explain the steady increase of the impedance with frequency due to the addition of a reactive/imaginary component to the real part of Z. Such stray inductance can be simulated and then the impedance corrected accordingly.



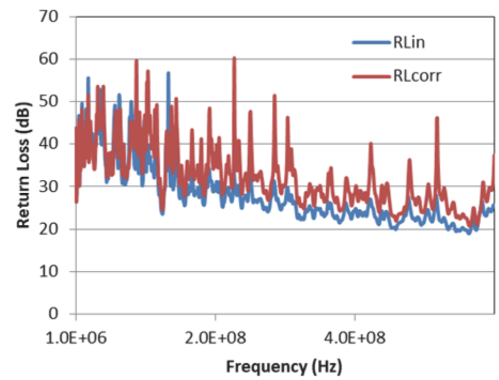


Figure 5: Measured and corrected for parasitic inductance impedance and return loss

Both the impedance and the RL prior (in blue) and after parasitic inductance correction (in red) are illustrated in Figure 5. In our case, the correction effect is negligible. This could be explained either by a low stray inductance (i.e. sound cable connection to the interface) and/or potentially by adequate zero correction at the cable calibration plan.

4.3 Fitted return loss (IEC 61156-1-5)

The fitted return loss correction procedure relies on transmission line theory in which the impedance converges asymptotically at high frequency (see Figure 1). Deviation from this asymptotic value is being mathematically corrected by fitting procedures according to the following steps:

1. First, the measured impedance curve is fitted with the least square regression method using below function with 2 unknown coefficients only:

$$Z_{fit} = K_0 + \frac{K_1}{\sqrt{f}} \quad (6)$$

   Assuming that high frequency values are less representative of the real properties of the DUT, the fit is performed up to a f_{max} of few hundreds MHz.

2. Second, we calculate the difference between the measured and fitted curves. It represents the variations

that are assumed to be spurious effects without physical relevance.

3. Third, these variations are least square fitted using a polynomial of degree n (n equal to 6 in our case based on empirical study).

4. Fourth, we subtract this polynomial fit from the original measured data to obtain the corrected impedance and return loss, respectively.

The corresponding impedance and return loss before (measured) and after correction (corrected) are shown in Figure 6:

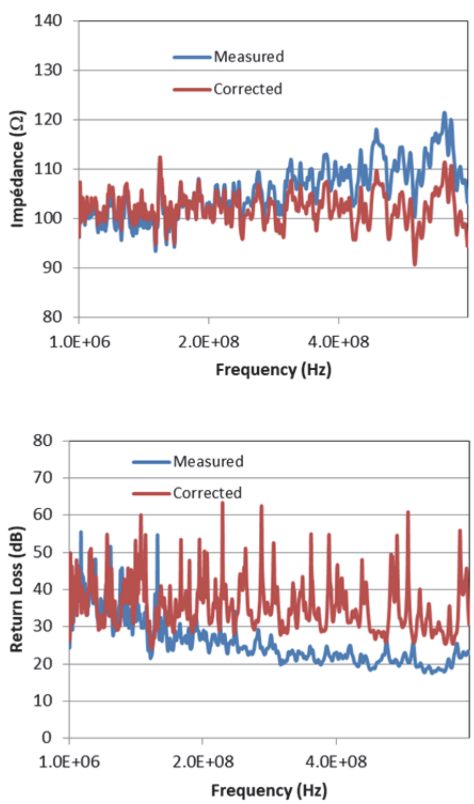


Figure 6: Measured and corrected impedance following the fitted return loss correction procedure

We notice that after correction, the impedance plot is closer to the expected result and the so-called abnormal behaviour is partially removed. Nonetheless, we need to ask ourselves if this multi-steps quite complex procedure is not too arbitrary and if these mathematical fits do have a real physical significance.

5. Time Domain Analysis

5.1 Gated Return Loss (IEC 61156-1-5)

Any defects or impedance mismatches will induce reflections in the measured DUT frequency response. By using a TDR (Time Domain Reflectometer), these anomalies will translate into well localised peaks in the time domain. However, unlike a VNA with narrowband receivers, a TDR uses a wideband filter leading to poor signal to noise ratio. Therefore, the high dynamic range of an ATE presents major advantages over a TDR in performing test measurements in both frequency and time domains.

Time gating is a well-known signal analysis method used to isolate a single response in time and consequently in space knowing the propagation constant. For cable measurement, it consists in the following steps:

1. measuring first in the frequency domain

2. performing an inverse DFT (discrete Fourier transformation) to move into the time domain

3. using a “gate” to artificially eliminate peaks in the time spectrum

4. applying DFT to convert back into frequency domain

The norm or absolute value of the S11 parameter in the time domain is plotted in Figure 7. The horizontal axis was converted to the cable length using a propagation constant of ~70% of the speed of light in vacuum, c_0. The blue, green, and red curves correspond to raw $|S_{11}|$, the applied gate, and the resulting gated $|S_{11}|$, respectively.

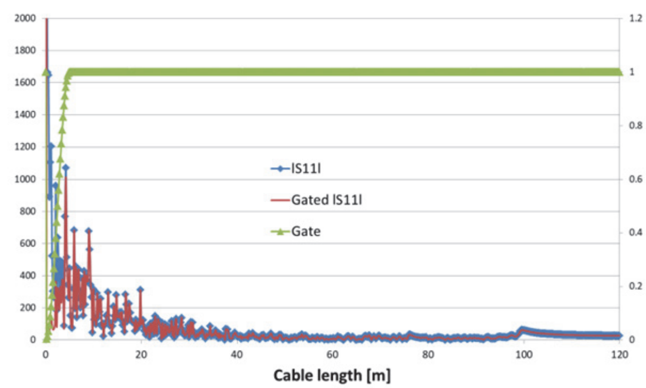
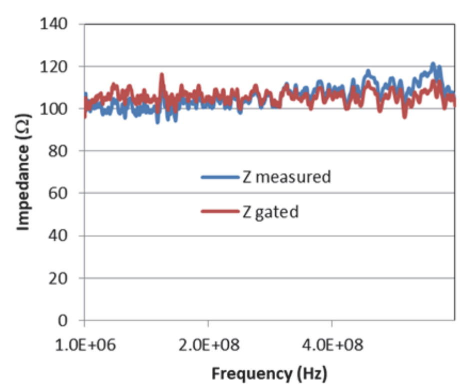


Figure 7: S_{11} parameter in the time domain

The then calculated impedance and RL plots before and after gating are shown in Figure 8.

On the impedance plot, the slight increase of Z with frequency is removed following signal gating. Similarly, the return loss flattens but still gets worse at lower frequency after gating correction.



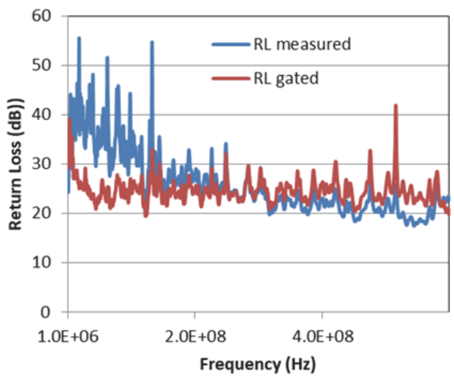


Figure 8: Measured and gated impedance and return loss

5.2 Time Domain Evaluation

As highlighted in the previous paragraph, it could be very useful to interpret the data in the time-domain directly. For instance, it allows checking the value of the impedance over the length of the cable, verify the exact cable length (knowing the velocity of propagation), control the presence of the connectors, identify localized defects, etc …

At AESA we have developed a fully automated procedure to do time domain analysis. This procedure is implemented in our ATE, performing frequency measurement and switching to time domain using Fourier transformation. A practical example for a 3.5m long coaxial jumper cable is given in Figure 9, for frequencies up to 6GHz.

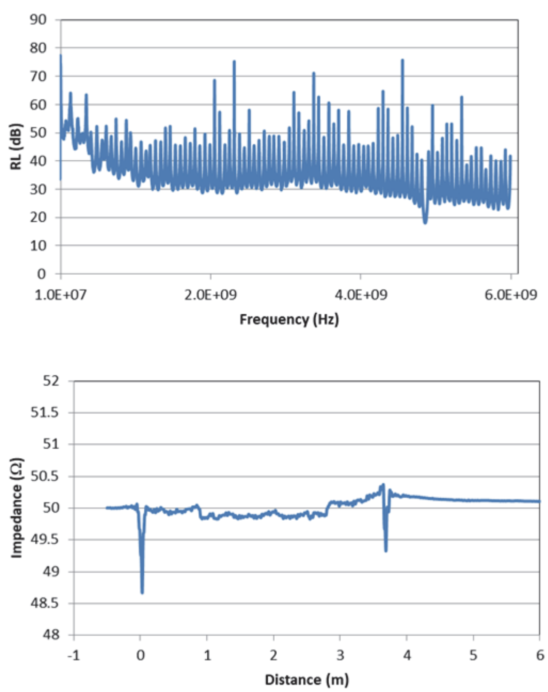


Figure 9: Measured return loss on a short (3.5m) coaxial cable and its corresponding TDR

The TDR plot shows the position of the connectors (at 0m and 3.5m) along with the impedance value of the cable. As the VNA does not go down to DC value, the Fourier transformation does not provide the exact value of the impedance and we must do some adjustment towards the known 50Ω .

6. De-embedding

As previously mentioned, cable test fixtures render the measurement analysis difficult. Therefore, de-embedding of these latter is another tool to suppress their effects. This can be done by extracting the S-matrix of the test fixtures, from measurement and/or electromagnetic (EM) simulation (the S-parameters being the elements of the S-matrix).

However, although very convenient to describe an n-port system, the S-matrix is not well suited to characterize the response of a cascaded system. To do so, we use the T-matrix representation, which directly relates the EM waves on the input(s) and output(s). For a cascaded system, the resulting T-matrix is the multiplication of its individual T-matrices components, from "left" to "right".

Considering a two test fixtures A and B at the cable near and far end, respectively, then:

$$[T_{measured}] = [T_A][T_{Cable}][T_B] \tag{7}$$

Hence

$$[T_{Cable}] = [T_A]^{-1}[T_{measured}][T_B]^{-1} \tag{8}$$

After correction, T-parameters are converted back to S-Parameters for evaluation of the cable properties. The conversion formula from S to T matrix and vice versa can be found in the literature.

In summary, the de-embedding process permits to mathematically de-embed the frequency response of test fixtures from the cable itself. It relies on a complete characterization of the test fixtures over the full frequency range of interest.

7. Conclusions

In this paper we discussed the challenges of characterizing a DUT/cable using an ATE that encompasses multiple sub-systems, including VNA, test fixtures, interfaces, etc... . Whereas the principal objective is to assess the cable's intrinsic properties, these sub-systems exert influence on the overall measurement.

Consequently, we reviewed various procedures to alleviate unwanted effects and perturbations from cable preparation, in order to better match experimental data with theoretical predictions. In addition, we demonstrated the relevance of doing some time analysis for better identifying and localizing defects.

Nonetheless, these correction procedures use mathematical schemes that could be quite remote from a well-defined physical framework.

Moreover, measurements accuracy strongly depends on calibration procedures. Consequently, as future research activities we propose to further work on the development of:

- Well-defined artefacts for performing the zero correction just prior to the cable fixture
- Full EM modelling of the cable test fixtures towards de-embedding

8. References

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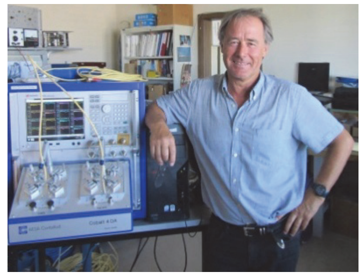
9. Authors

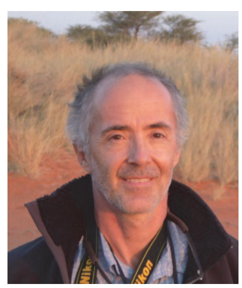
Laurent Van Rysselberghe joined AESA in March 2019 as R&D project manager in the field of automatic test equipment. He owns a Bachelor of Science in Electrical Engineering from the Ecole d'Ingénieurs de l'Etat de Vaud in Yverdon HEIG-VD). He had previously worked for 20 years within the cable manufacturing group Nexans. At Nexans, he occupied various positions in high voltage, optical fibres or CATV/radiating cable families as R&D engineer, operational quality manager and production manager of the Cortaillod production plant. He then evolved into the technical expert ladder in electrical performances and testing.

Wolfgang Klein holds a degree of Dipl.-Ing. (TH) Information Technology from RWTH Aachen University (Germany). During and after his university education he worked in the testing department of the German cable manufacturer Kerpenwerk. His responsibilities connected with central IT were related to networking and automating test equipment. In 1994, he joined M.E.A. (Mauf und Rudow) where he used his practical experience to design the Quality Management System CIQ 3.0. He also developed the foundation of some modern telecom automatic test equipment such as the balunless data cable measurement systems "Cobalt". Since the merger of M.E.A. and AESA, he continues his role as head of the System Development Department.



Dick Gigon received his Microelectronic Engineering diploma in Neuchatel University and Ecole Polytechnique Fédérale de Lausanne (EPFL) in 1978. After 10 years in CMOS/TTL chip design and micro packaging technologies in Switzerland and USA, he joined AESA in May 1991 as Lab supervisor and telecom test equipment designer for copper and fibre optic cables. Specialist in RF passive components, baluns, filter, HF multiplexers, he has a significant experience in testing telephone, DSL, data LAN and coaxial cables to 6 GHz.

Boris Dardel obtained his PhD in physics in 1994 at the University of Neuchatel (Switzerland) in Condensed Matter Physics. He then joined the cable manufacture of Nexans Suisse SA in Cortaillod (Switzerland) where he managed different technical departments linked with materials, cable designs, testing and R&D. In 2016, Dr. Dardel came to AESA SA in Colombier (Switzerland) as R&D Manager, responsible for designing and leading R&D processes, specifically linked to the measurement of electrical resistance for energy cables.



Vincent Arbet-Engels is the CEO/Managing Director of AESA, a leading manufacturer of test equipment for the cable industry. Prior to AESA, he held various scientific and management positions at CERN, IBM, and Abilis Systems, in both the USA and Europe.

Dr Arbet-Engels graduated from the University of California, Los Angeles (UCLA) in 1992, with a Ph.D. in Electrical Engineering. He also earned a M.S. from UCLA, as well as a M.S. and B.S. from the Swiss Federal Institute of Technology in Lausanne (EPFL) in Microengineering.